CLAIMS AS PENDING FOR U.S. PATENT

APPLICATION NO. 09/625,071

11. A lead frame panel suitable for forming an array of integrated circuit packages for accommodating a semiconductor die, the lead frame panel having an array of device areas, each device area being suitable for forming an independent integrated circuit package and comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads, wherein the plastic encapsulation is part of a molded cap that covers an array of the device areas.

12. An integrated circuit package as in Claim 11, further comprising a solder ball attached to each of said exposed lower surface of said conductive leads.

13. An integrated circuit package for accommodating a semiconductor die, comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads, and

wherein said integrated circuit package is ~~one~~ a two dimensional matrix array of a plurality of integrated circuit packages fabricated simultaneously on said lead frame, said lead frame comprising a two dimensional array of die attach pads and conductive leads that are positioned under the plastic encapsulation, and wherein said adhesive pad supports the array of die attach pads and conductive leads prior to singulation of the plurality of integrated circuit packages.

15. An integrated circuit package as in Claim 13, wherein said lead frame is fabricated on a metal panel.

16. An integrated circuit package for accommodating a semiconductor die, comprising:

a planar lead frame fabricated on a metal panel comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads,

wherein said integrated circuit package ~~is one~~ a two dimensional matrix array of a plurality of integrated circuit packages fabricated simultaneously from said lead frame, said lead frame comprising an array of die attach pads and conductive leads, and said adhesive pad supports said die attach pads and said conductive leads prior to singulation of said plurality of integrated circuit packages and

further comprising an encapsulant dam provided to enclose said array of die attach pads and conductive leads.

17. An integrated circuit package as in Claim 13, wherein said array of die attach pads and conductive dies is being arranged in a regular pattern so as to allow singulation of said integrated circuit packages by sawing through said plastic encapsulation and said conductive leads at predetermined positions.

18. A lead frame panel suitable for use in packaging an array of integrated circuits, the lead frame panel being formed from a conductive sheet and having top and bottom surfaces, the lead frame panel comprising:

a matrix of tie bars that extend in substantially perpendicular rows and columns to define a two dimensional array of immediately adjacent device areas separated only by

the tie bars, each device area being suitable for use in an independent integrated circuit package;

a multiplicity of die attach pads; and

a multiplicity of conductive contacts, the conductive contacts being mechanically carried by the tie bars; and

wherein each device area includes one of the die attach pads and a plurality of the conductive contacts that are positioned generally adjacent the die attach pad.

19. A lead frame panel as recited in claim 18 wherein the die attach pads, the conductive contacts and the tie bars are all substantially co-planar.

20. A lead frame panel as recited in claim 19 wherein the conductive contacts and the die attach pads are substantially the same thickness.

21. A lead frame panel as recited in claim 18 further comprising an adhesive tape adhered to a bottom surface of the lead frame panel.

22. A panel assembly of integrated circuits comprising:

a lead frame panel as recited in claim 18;

a plurality of dice, each die being carried by an associated die attach pad; and

a molded cap that covers the array of device areas while leaving bottom surfaces of the die attach pads and the conductive contacts exposed, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel assembly.

23. A packaged integrated circuit formed by singulating the panel assembly recited in claim 22, wherein the conductive contacts in the packaged integrated circuit do not extend beyond the edge of the encapsulation material in the packaged integrated circuit and the die attach pad in the packaged integrated circuit is exposed.

24. A packaged integrated circuit as recited in claim 23 wherein the conductive contacts and the die attach pad are substantially the same thickness.

25. A panel assembly as recited in claim 22 further comprising an adhesive tape adhered to a bottom surface of the lead frame panel, whereby the adhesive tape serves to keep the exposed surface of the exposed encapsulation material substantially co-planar with the bottom surfaces of the contacts and die attach pads.

26. A panel assembly suitable for use in packaging an array of integrated circuits simultaneously, the panel assembly having top and bottom surfaces and comprising:

a lead frame panel formed from a conductive sheet, the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas, each device area being suitable for use as part of an independent integrated circuit package and including a die and a plurality of contacts positioned around and electrically connected to the die; and

a molded cap that substantially uniformly covers the array of device areas while leaving bottom surfaces of the conductive contacts exposed to facilitate electrical connection to external components, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel of integrated circuits to physically isolate the contacts.

27. A panel assembly as recited in claim 26 wherein:

each device area in the lead frame panel further includes a die attach pad; and

bottom surfaces of the die attach pads are also exposed.

28. A panel assembly as recited in claim 27 wherein the die attach pads, the conductive contacts and the tie bars are all substantially co-planar.

29. A panel assembly as recited in claim 28 wherein the conductive contacts and the die attach pads are substantially the same thickness.

30. A panel assembly as recited in claim 26 further comprising an adhesive tape adhered to a bottom surface of the lead frame panel, whereby the adhesive tape serves to

keep the encapsulation material exposed at the bottom of the panel assembly substantially co-planar with the bottom surfaces of the contacts and die attach pads.

31. A panel assembly as recited in claim 26 further comprising bonding wires for electrically coupling the dice to their associated contacts, wherein the molded cap encapsulates the bonding wires.

32. A packaged integrated circuit formed by singulating the panel assembly recited in claim 26, wherein the conductive contacts in the packaged integrated circuit do not extend beyond the edge of the encapsulation material that is part of the packaged integrated circuit.

33. A packaged integrated circuit as recited in claim 32 wherein the integrated circuit is singulated by sawing the panel assembly along substantially perpendicular lines.

38. A panel assembly suitable for use in packaging an array of integrated circuits, the panel assembly having top and bottom surfaces and comprising:

a lead frame panel formed from a conductive sheet, the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas, each device area being suitable for use as part of an independent integrated circuit package and including a plurality of contacts;

a plurality of dice, each die being associated with one of the device areas and being electrically connected to the associated contacts; and

a molded cap that covers the array of device areas while leaving bottom surfaces of the contacts exposed to facilitate electrical connection to external components, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel of integrated circuits to physically isolate the contacts; and

an adhesive pad adhered to a bottom surface of the lead frame panel, whereby the adhesive pad serves to keep the encapsulation material exposed at the bottom of the panel assembly substantially co-planar with the bottom surfaces of the contacts and die attach pads.

39. A panel assembly as recited in claim 38 wherein:
each device area in the lead frame panel further includes a die attach pad; and
bottom surfaces of the die attach pads are also exposed.

40. A panel assembly as recited in claim 39 wherein the lead frame panel further comprises tie bars that support the contact, wherein the device areas are substantially immediately adjacent one another with only the tie bars residing therebetween.

41. A panel assembly as recited in claim 40 wherein the die attach pads, the contacts and tie bars are all substantially co-planar.

42. A panel assembly as recited in 39 wherein the conductive contacts and the die attach pads are substantially the same thickness.

43. A panel assembly as recited in claim 38 further comprising bonding wires for electrically coupling the dice to their associated contacts, wherein the molded cap encapsulates the bonding wires.

44. A packaged integrated circuit formed by singulating the panel assembly recited in claim 38, wherein the contacts in the packaged integrated circuit do not extend beyond the edge of the encapsulation material that is part of the packaged integrated circuit.